(12) UK Patent Application (19) GB (11) 2 138 206 A

(43) Application published 17 Oct 1984

(21) Application No 8404567

(22) Date of filing 21 Feb 1984

(30) Priority data

(31) 58/027748 (32) 23 Feb 1983 (33) JP

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(51) INT CL[3]
H01L 29/92 27/10 // 29/94

(52) Domestic classification
H1K 11B3 11C1A 11C4 11D1 11D 1FE 1FF 4C11 4C14 4C2B 4C2D 5E9 9D1 FE FF GAX
U1S 2099 H1K

(56) Documents cited
GB A 2092825
GB A 2092372
GB A 2060250
GB 1564617
GB 1254899
GB 1133634
EP A1 0058998

(58) Field of search
H1K

(54) Variable capacitor element

(57) The variable capacitor element comprises a depletion layer control means (16A,16B) formed on a semiconductor substrate (11) and a capacity read-out means including a capacity read-out electrode (24) and formed on the semiconductor substrate via a spacing of an insulative layer (14). The element is particularly characterized in that a surface potential of the semiconductor substrate underbeneath the capacity read-out electrode (22) is stored, so that a resulting capacity appearing at the capacity read-out means in response to a bias voltage applied to the depletion layer control means represents one of stabilized large and small values.

FIG. 4 (a)

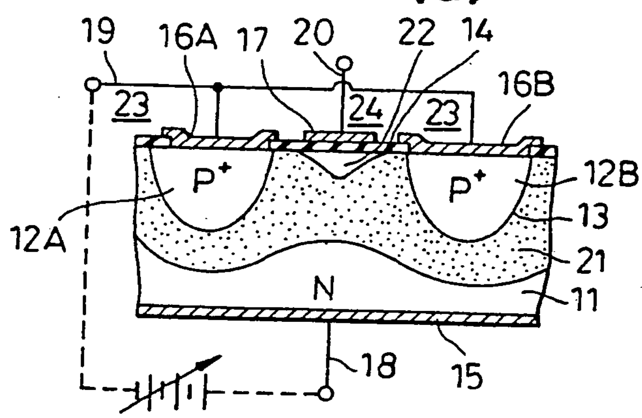

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FIG. 1
PRIOR ART

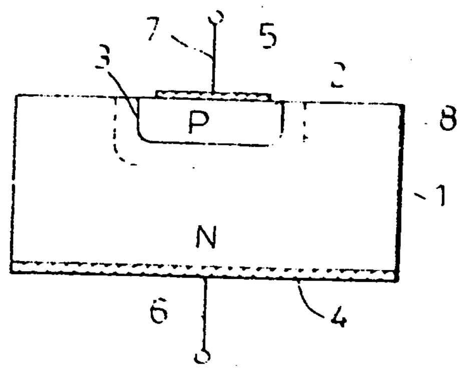


FIG. 5

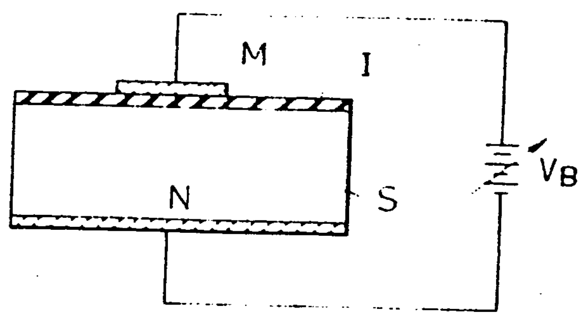


FIG. 6

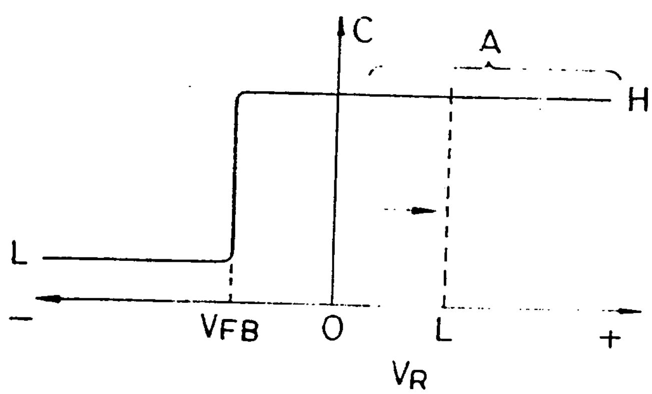


FIG. 2 (a)

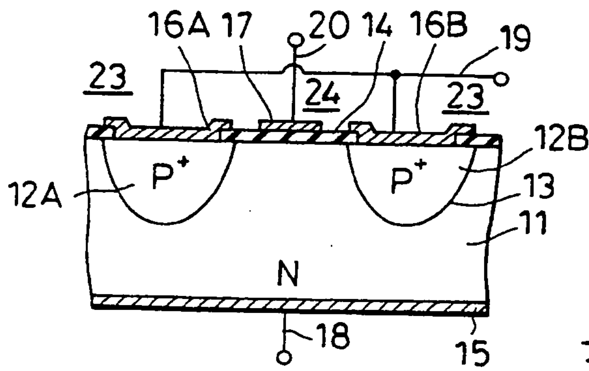


FIG. 2 (b)

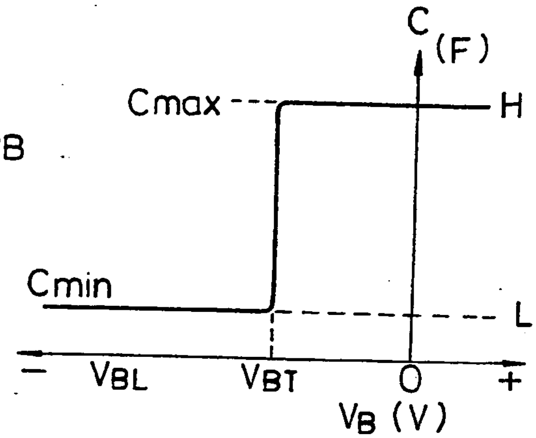


FIG. 3 (a)

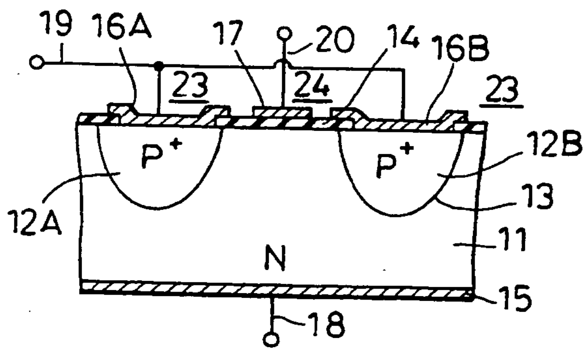


FIG. 3 (b)

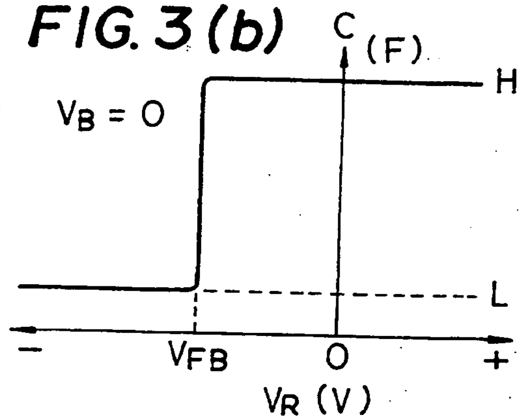


FIG. 4 (a)

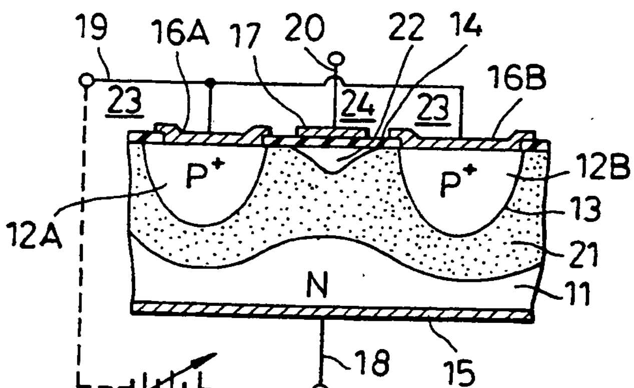


FIG. 4 (b)

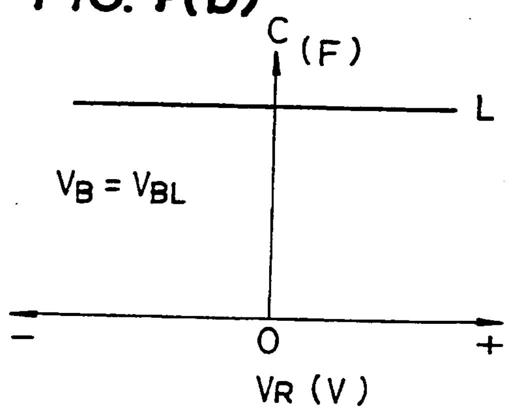
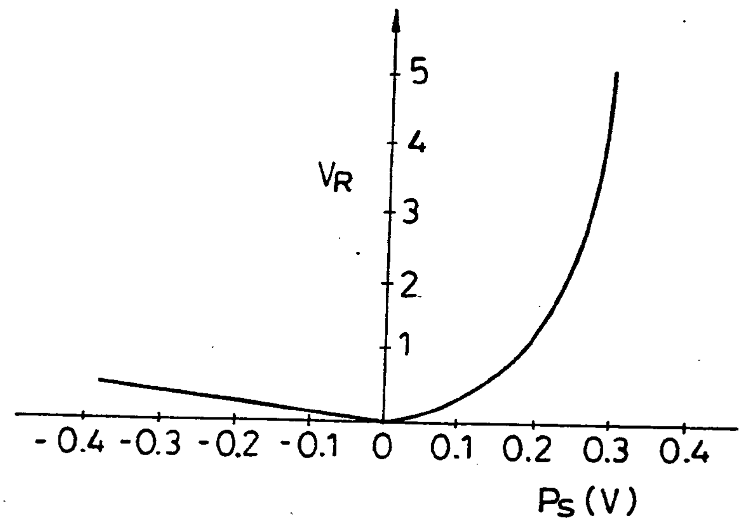
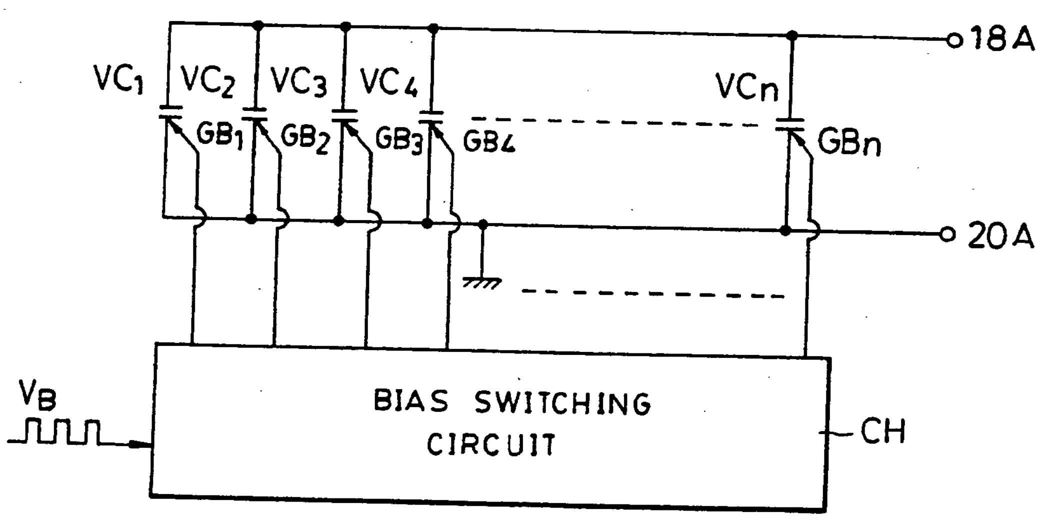


FIG. 7



5
4
V_R
3
2
1
- 0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
Ps (V)

FIG. 8



18A
20A
VC_1
VC_2
VC_3
VC_4
VC_n
GB_1
GB_2
GB_3
GB_4
GB_n
V_B
BIAS SWITCHING
CIRCUIT
CH

FIG. 9 (a)

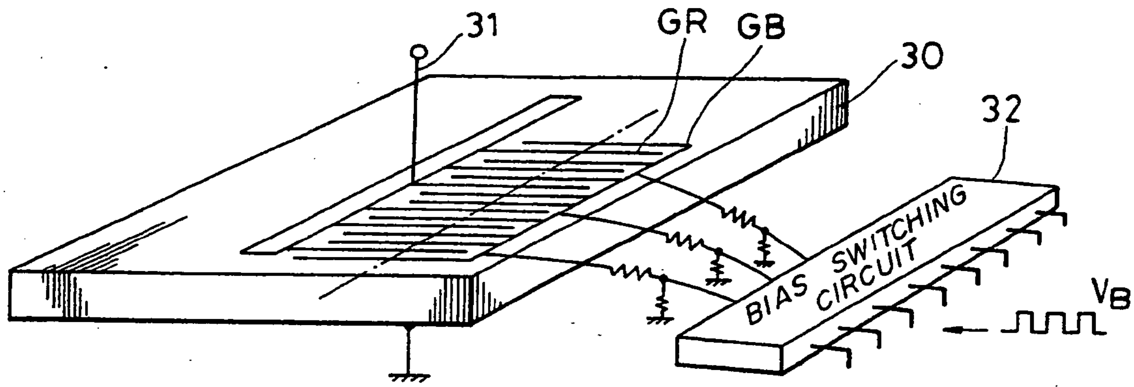


FIG. 9 (b)

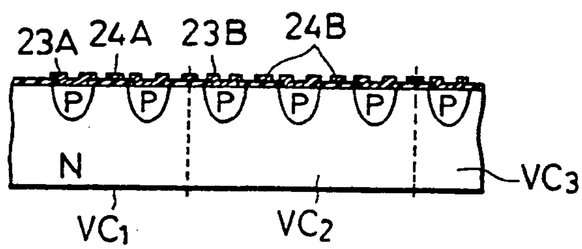
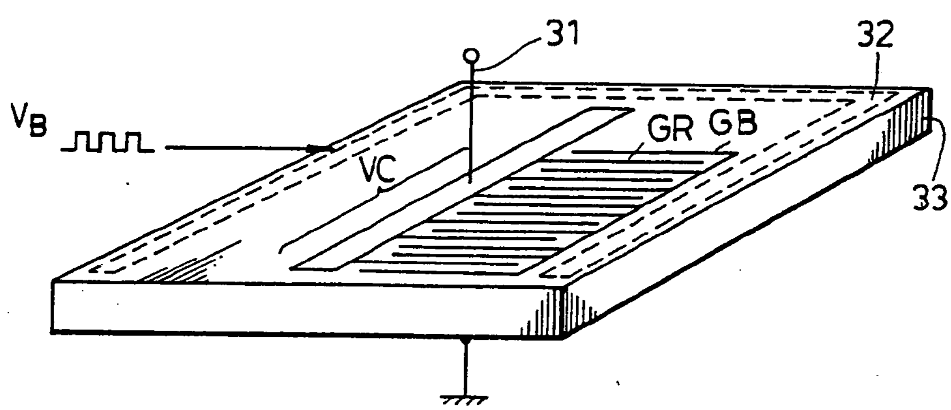


FIG. 10



SPECIFICATION

Variable capacitor element

This invention relates to a variable capacitor element particularly improved to reduce capacity fluctuation depending on potentials of input signals.

One of prior art variable capacitor elements uses a pn junction diode as shown in Figure 1. In the Figure, reference numeral 1 is an n-type semiconductor region, 2 is a p-type semiconductor region, 3 is a pn junction, 4 and 5 are ohmic electrodes attached to the n- and p-type regions 1 and 2 respectively, 6 and 7 are lead terminals derived from the ohmic electrodes 4 and 5 respectively, and 8 is a depletion layer.

The depletion layer 8 changes its volume in accordance with a bias voltage applied to the lead terminals 6 and 7 so that a capacity corresponding to the volume of the depletion layer 8 is detected between the terminals 6 and 7.

The prior art element, however, uses the lead terminals 6 and 7 as both the capacity read-out terminals (electrode) to pick up the resulting capacity and the bias terminals to change the volume of the depletion layer 8. Therefore, the depletion layer 8 changes its volume not only with application of a bias voltage but also with application of an input signal between the lead terminals 6 and 7, thereby causing fluctuation of a resulting capacity. If this capacitor element is employed in a tuning circuit, such a fluctuation of the resulting capacity causes tuning errors and deteriorations of the cross modulation characteristic. More specifically, the resulting capacity is fluctuated by potentials of inputs signals applied to the element, and moreover, this fluctuation is not linear. This means that such input signals are frequency modulated, and high frequency components other than the input signals themselves appear in the output accordingly.

Therefore, the prior art variable capacitor element involves various problems as follows:

(1) a resulting capacity is greatly affected by potentials of input signals;

(2) the two-way use of electrodes as the capacity readout electrode and as the bias electrodes does not allow free selection of designs of circuit arrangement;

(3) since the capacity variation depends on the carrier density of a semiconductor region of the element, the variation cannot be increased so much; and

(4) due to various restrictions in the manufacturing process of the element, it is difficult to integrate the element together with other RF and IF circuit elements on a single substrate.

It is therefore an object of the invention to provide a variable capacitor element whose capacity is hardly affected by input signals and instead determined merely by bias voltages.

So as to attain the object and overcome the problems involved in the prior art, the invention provides a variable capacitor elem nt comprising a depletion layer control means and a capacity read-out means having a capacity read-out electrode which both means are formed on a semiconductor substrate and spaced by an insulative layer, the element being particularly characterized in that the surface potential of the semiconductor substrate underbeneath the capacity read-out electrode is stored so that a capacity appearing at the capacity read-out means in response to a bias voltage applied to the depletion layer control means can represent only two stabilized values, large and small.

The invention will be better understood from the description hereunder made by way of the preferred embodiments illustrated.

Figure 1 is a cross sectional view of a prior art variable capacitor element;

Figures 2a, 3a, 4a and *5* are cross sectional views of variable capacitor elements embodying the invention;

Figures 2b, 3b, 4b, 6 and *7* show characteristics of the elements shown by Figures 2a, 3a, 4a and 5, respectively;

Figure 8 is a circuit arrangement of a variable capacitor device comprising plural variable capacitor elements according to the invention;

Figure 9a is a perspective view of a plurality of variable capacitor elements according to the invention integrated on a semiconductor substrate;

Figure 9b is a cross sectional view of the structure shown by Figure 9a; and

Figure 10 is a perspective view of an integrated circuit wherein plural variable capacitor elements according to the invention and a switching circuit element therefor are integrated on a single semiconductor substrate.

Figures 2a and 2b to 4a and 4b are cross sectional views and characteristic graphs of MIS-type variable capacitor elements selected for explanation of the invention. Reference numeral 11 designates an n-type semiconductor region of a semiconductor substrate. The substrate also includes p+ conductor regions 12A and 12B. Reference numerals 13 denotes pn junctions between the n-type semiconductor region 11 and the p+ conductor regions 12A and 12B. An insulative layer 14 is formed on the n-type semiconductor region 11 to bridge the p+ regions 12A and 12B. The n-type region 11, the both p+ regions 12A and 12B and the insulative layer 14 individually have their electrodes 15, 16A, 16B and 17. Lead terminals 18, 19 and 20 are derived from the electrodes 15, 16A, 16B and 17, respectively. In Figure 4a, a depletion layer 21 is produced along the pn junctions 13, reserving a residual storing layer 22 not involved in the depletion layer underbeneath the insulative layer 14. The p+ regions 12A and 12B and the electrodes 16A and 16B thereof constitute a depletion layer control means 23 whereas the insulative layer 14 and the electrode 17 thereof make a capacity read-out means 24.

The MIS-type variable capacitor element of Figure 2a, which is also disclosed by a Japanese Patent Application officially published under discl sure number 120178/1980, is adapted so that the depletion layer 21 changes its volume in response a bias voltage V_B applied between the lead terminals 18 and 19 for reverse biasing the pn junctions 13, and a resulting capacity corresponding to the volume of

the depletion layer 21 is picked up between the lead terminals 18 and 20. The relation between the capacity C and the voltage V is shown by Figure 2b, wherein the capacity H is the value obtained when the reverse bias voltage V_B is zero, and the capacity L is the value obtained when the reverse bias voltage V_B is increased to an extent V_{BL} exceeding the threshold voltage V_{BT}. The capacities H and L represent the maximum capacity C_{max} and the minimum capacity C_{min} respectively in this MIS.C-V characteristic.

When the reverse bias voltage V_B between the lead terminals 18 and 19 is zero, and the bias voltage V_R between the lead terminals 18 and 20, i.e. the voltage to the capacity read-out electrode 17 is increased or decreased, the C-V characteristic as shown by Figure 3b is obtained. This is substantially same as the general MIS.C-V characteristic of Figure 2b. It is evident therefore that if the bias voltage V_R to the capacity read-out electrode 17 is varied while the bias electrodes 16A and 16B are not biased, the same MIS.C-V characteristic as shown by Figure 2b is obtained.

If the bias voltage V_R between the lead terminals 18 and 20 is varied while the reverse bias voltage V_{BL} is applied between the lead terminals 18 and 19 as shown by Figure 4a, the C-V characteristic as shown by Figure 4b is obtained. As understood from this C-V characteristic, when the reverse bias voltage V_{BL} is selected so as to sufficiently stabilize the capacity C at the value L, displacement of the bias voltage V_R in the plus or minus direction about the zero point does not cause substantial changes of the capacity C and instead keeps it at the value L.

On the other hand, the C-V characteristic of Figure 3b represents a change in capacity when the bias voltage V_R varies in one direction and exceeds a point V_{FB}. It is therefore evident that the capacity depends on the bias voltage V_R.

This means that the variable capacitor element having the above-described construction as it is suffers capacitor fluctuations due to input signals applied to the capacity read-out electrode 17.

With the MIS-type variable capacitor element as shown by Figure 5, assume now that the semiconductor substrate S has an n-type conductivity. If a considerable large bias voltage V_B is applied to an electrode M via an insulator I, a number of electrons gather along the MIS interface between the insulator I and the semiconductor substrate S, so that the surface potential is stored. Reference A in the C-V characteristic of Figure 6 designates the state that the surface potential is stored. In this state, the capacity C is maintained at the value H. While the surface potential is stored, the potential designated by reference Ps varies by an extremely small amount with respect to variation of the bias voltage V_R to the capacity read-out electrode, as shown by the graph of Figure 7 which is conducted from the MIS theory. It is therefore evident that inspite a variation of the bias voltage V_R the capacity fluctuation is kept very small provided the variation is given while the surface potential is stored.

This invention employs this phenomenum and provides a variable capacitor element capable of storing the surface potential along the MIS interface, thereby producing a resulting capacity which is not affected by a voltage applied to the MIS electrode and is instead stabilized at a large or small value H or L.

One of preferable means for storing surface potential is biasing the capacity read-out electrode 17 so as to a previously storing the surface potential, as shown in Figure 5.

Second means is an ion implantation of donor impurities such as arsenic (As), phosphorus (P) or antimony (Sb) into the superficial area of the n-type semiconductor region underbeneath the capacity read-out electrode 17. If the semiconductor region 11 has a p-type conductivity, acceptor impurity ions are implanted. Thereby, positive or negative ions are generated along the MIS interface.

From a view point of a potential difference between the capacity read-out electrode 17 and the bias electrodes 16A and 16B, the second means will be better because the first means is likely to suff r a Q change due to a charge leakage through the insulator I.

By storing the surface potential along the MIS interface, the zero bias point in the C-V characteristic may be substantially displaced to the position L in the right in Figure 6, so that the bias voltage V_R is varied in both the plus and minus directions about the L point. Accordingly, the variable range of the bias voltage V_R keeping the capacity C at the value H is largely increased to an extent not exceeding the voltage V_{FB}, thereby eliminating dependency of the capacity C on the bias voltage V_R.

It is therefore evident that by storing the surface potential along the MIS interface, and by selecting the bias voltage between the bias electrodes 16A and 16B at zero or at a value larger than the threshold value V_{BT}, the resulting capacity represents the stabilized large or small value H or L, correspondingly.

The maximum and minimum capacities C_{max} and C_{min} corresponding to the values H and L of the MIS-type variable capacitor element as shown by Figures 2 to 4 can be selected as desired by varying parameters of materials consisting the MIS structure. For example, changes in carrier density and volume of the semiconductor regions 11, 12A and 12B, thickness of the insulative layer 14, dimension of the electrode 17, or some other factors will allow a desired selection of the values H and L.

Figure 8 shows a plurality of such MIS-type variable capacitor elements VC_1, VC_2, VC_3 ..... having different H and L values and parallelly connected. Bias electrodes GB_1, GB_2, GB_3 ..... of the respective elements are connected to a bias switching circuit CH, so that a desired one of the bias electrodes is selected by the switching circuit CH and is supplied with a bias voltage V_B to obtain a desired resulting C-V characteristic between the capacity read-out electrodes 18A and 20A. For example, if nine to tw lve l m nts with different H and L values are combined by a logical circuit used as th switching circuit CH, various C-V characteristics can be obtained within an accuracy 1 to 0.1 pF.

Figure 9a shows said plural MIS-type variable

capacitor elements VC_1, VC_2, VC_3 ..... integrated on a semiconductor substrate 30. The capacity read-out electrodes GR_1, GR_2, GR_3 ..... of the respective elements are commonly connected to a lead terminal 31. The bias electrodes GB_1, GB_2, GB_3 ..... are individually connected to a bias switching circuit 32 so as to be independently supplied with the bias voltage V_B. Figure 9b is a cross sectional view of the integrated structure of Figure 9a. Reference numerals 23A and 23B designate depletion layer control means, and reference numerals 24A and 24B denote capacity read-out means.

Figure 10 illustrates a construction wherein the variable capacitor elements VC and the switching circuit 32 are integrated together on a single semiconductor substrate 33.

The semiconductor regions of the element may be selected to be p-type, or n-type as desired.

As will be understood from the aforegoing description, the invention overcomes various problems involved in the prior art element because in the variable capacitor element comprising the depletion layer control means and the capacity read-out means including the capacity read-out elecrode both formed on a semiconductor substrate and spaced by an insulative layer, a surface potential of the semiconductor substrate underbeneath the capacity read-out electrode is stored so that a capacity appearing at the capacity read-out means represents one of stabilized large and small values in response to a bias voltage applied to the depletion layer control means.

Summarizing advantages of the invention,

(1) since a resulting capacity is not affected by potentials of input signals, the capacity represents an accurate value determined merely by a bias voltage,

(2) since the capacity read-out electrode and the bias electrode are independent from each other, a relatively free selection of circuit arrangements is allowed,

(3) the capacity variation range can be increased, and

(4) the elements can be readily integrated together with other circuit elements on a single substrate.

In particular, substantial independency from input signals applied to the capacity read-out electrode leads to prevention of tuning errors and prevention of generation of high frequency components, thereby improving the cross modulation characteristic.

CLAIMS

1. A variable capacitor element which comprises:

a semiconductor substrate;

depletion layer control means formed on said substrate;

an insulative layer formed on said substrate;

capacity read-out means formed on said insulative layer;

surface potential storing means to store the surface potential in said semiconductor substrate underbeneath said capacity read-out means; and

bias voltage applying means for applying a bias voltage to said depletion layer control means so that a capacity appearing at said capacity read-out means represents one of stabilized large and small values.

2. A variable capacitor element as set forth in Claim 1 wherein said surface potential storing means comprises means for biasing said capacity read-out means so as to previously store said surface potential.

3. A variable capacitor element as set forth in Claim 1 wherein said semiconductor substrate has an n-type conductivity, and said surface potential storing means comprises an ion implantation of donor impurities into said n-type semiconductor substrate underbeneath said capacity read-out means.

4. A variable capacitor element as set forth in Claim 1 wherein said semiconductor substrate has a p-type conductivity, and said surface potential storing means comprises an ion implantation of acceptor impurities into said p-type semiconductor substrate underbeneath said capacity read-out means.

5. A variable capacitor element which comprises:

a semiconductor substrate;

a plurality of depletion layer control means formed on said semiconductor substrate and connected to each other;

a plurality of capacity read-out means formed on said substrate and spaced from said substrate by an insulative layer;

surface potential storing means for storing the surface potential within said semiconductor substrate underbeneath said respective capacity read-out means; and

bias switching means for selectively applying a bias voltage to said depletion layer control means.

6. A variable capacitor element as set forth in Claim 5 wherein said bias switching means is formed on said semiconductor substrate.

7. A variable capacitor element substantially as herein described with reference to Figures 2 to 10.

Printed in the UK for HMSO, D8818935, 8/84, 7102.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.